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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,555	03/22/2001	David B. Squires	X-857 US	6451

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
HUYNH, KIM NGOC	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,555	SQUIRES, DAVID B.	
	Examiner	Art Unit	
	Kim Huynh	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10-13 and 23-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-13. 23-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

■

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/18/05 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-6, 10, 23 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Akao (US 5,307,464).

a. Claims 1, 6, Akao discloses (Figs. 1-2 and 8-10) a system having menu allowing user to select one of a plurality of configurable logic devices (see Fig. 10), an integrated circuit 1 (see Figs. 1-2) having a bus 7-8 connecting a processor core 2 to a configurable peripheral device having a configurable logic block having circuitry capable

of implementing a plurality of logic functions (4-5) and the bus connecting the processor core 2 and the configurable device without a subprocessor (in the embodiment where 5 being PLA or PLD in place of coprocessor as discussed in col. 32, ll. 23-30 and col. 33, ll. 46-58) and a programmable routing matrix coupling to the logic block for routing the signals to and from the CLB (RAM array address control circuit for selecting column and row addresses, see at least Fig. 6 and 15).

b. Claims 2, 5, and 10, Akao discloses the configurable peripheral devices (peripheral functions) are versatile and can be of counter, timer, serial communication (UART), ROM, RAM (flash memory controller) (col. 1, l. 30-47).

c. Claim 4, Akao discloses the peripheral and bus are implemented on a FPGA (see Figs. 15-17 and 20). Please note memory arrays of Akao are field programmable and therefore meet the definition of FPGA. Akao suggested that his invention can be implemented using PLD or PLA (col. 32, ll. 27-32).

d. Claims 23, 28, Akao discloses a configurable I/O block 6 coupled to the configurable logic block to couple signals to/from an external device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 10-13, 23 and 28 are rejected under 35 U.S.C. 103(a) as being obvious over "The Programmable logic data Book 2000" in view of Akao (US 5,307,464).

a. Claims 1, 4, 6, 23 and 28, "The Programmable logic data Book 2000" discloses a Virtex-E FPGA device having all the feature of a CLB as claimed (programmable routing matrix, configurable I/O block and lookup table, see p. 3-7 to 3-12) for providing a high speed and high capacity programmable logic solution to enhance design flexibility (the Virtex_E FPGA is described in a printed publication and in public use/sale in this country, more than one year prior to the date of the instant application) and a configurable I/O block (Figs. 1-3) coupled to the configurable logic block to couple signals to/from an external device. It is inherent that the Virtex_E FPGA when in use would couple to a core processor via a bus in order to perform its function.

As for the limitation of using the FPGA to implementing the functions of peripheral devices, Akao discloses that it is well known in the art to implement a single chip microprocessor having embedded configurable hardware logic with a processor (CPU 2) to provide various peripheral functions (col. 1, ll. 29-65). It would have been obvious to one having ordinary skill in the art to utilize the Vertex_E FPGA in providing the peripheral functions in order to take advantage of a commercially available product which offers a high speed and high capacity programmable logic solution to enhance design flexibility of the peripheral device and allow the peripheral functions to be defined more easily and as defined by the user (Akao, col. 1, ll. 50-65).

Furthermore, please note recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

b. Claims 2, 5, and 10, Akao discloses the configurable peripheral devices (peripheral functions) are versatile and can be of counter, timer, serial communication (UART), ROM, RAM (flash memory controller) (col. 1, l. 30-47).

5. Claims 3, 11-13, 24-27 and 29-32 are rejected under 35 U.S.C. 103(a) as being obvious over Akao (per 35 USC 102 above) or "The Programmable logic data Book 2000" in view of Akao (per 35 USC 103 above) and further in view of applicant's admission (paragraphs 15-16).

Akao discloses all the limitations discussed above wherein the user can select the functions and characteristics of the specific of the UART function. Akao does not disclose the specific function of the UART being a baud rate generator. However, as admitted by applicant (Fig. 2A), the basic functions of a UART includes baud rate generator, modem control signal, RX-TX driver. Since Akao discloses the peripheral as being a configurable UART, it would have been obvious to one having ordinary skill in the art to include all the conventional functions of a UART in the configurable logic form in order to properly implement the intended peripheral device.

As for the specific user selectable options (baud rate, width size, and error correction selector); please note baud rate, width size, and error correction codes are property of a particular peripheral device to enhance its transmission operation. Since the combination of Akao and the Vertex_E FPGA above discloses a flexible and versatile system allowing the users to easily set and modify the peripheral functions in the his own way via programmable logic control (background and summary of the invention). Applicant admitted that the choice of user selectable options are various and can be tailored to meet the needs of the user; therefore, it would have been obvious to one having ordinary skill in the art to modify the system of Akao for the user to select options that is related to the peripheral being connected to the system based on the user's need and the operational specification of the peripheral device as intended Akao (col. 1, ll. 7-17).

Response to Arguments

Applicant's arguments filed 3/18/05 have been fully considered but they are not persuasive.

a. The examiner in the previous action requested a clarification as to what applicant defined as the structure of the "configurable logic block". In response, applicant defines the configuration logic block simply as something that provides functional elements for constructing logic and further argues that EPROM, RAM, PLD are programmable memory circuit or programmable logic device but are not configurable logic block (remark, pages 9-10). No details of the structure difference or

explanation as to why the EPROM, RAM, PLD differ from a "configurable logic block". It is unclear how something that provides function elements for constructing logic differs from EPROM, RAM, and PLD. Memory arrays are configurable (programmable) and include circuitry and capable of constructing logic which meet the definition of "configurable logic block". Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

b. As for the argument that the Akao reference teaches away from using hardware logic, please note that Akao discloses using a PLD in place of the coprocessor 5 in one of the embodiments (col. 32, ll. 23-30 and col. 33, ll. 46-58). MPEP 2131.05 [R-2] recites that a reference is no less anticipatory if, after disclosing the invention, the reference then disparages it. The question whether a reference "teaches away" from the invention is inapplicable to an anticipation analysis. Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998) (The prior art was held to anticipate the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed."). See also Atlas Powder Co. v. IRECO, Inc., 190 F.3d 1342, 1349, 51 USPQ2d 1943, 1948 (Fed. Cir. 1999) (Claimed composition was anticipated by prior art reference that inherently met claim limitation of "sufficient aeration" even though reference taught away from air entrapment or purposeful aeration.).

c. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicant argues against the combination of Akao with the Programmable Logic Data Book 2000 indicating that the Programmalbe Logic Data Book does not suggest using the configurable logic device for peripheral data. As discussed in the rejection, Akao discloses in the background the motivation and reasons and indicated that it is a common practice to use programmable logic device in implementing configurable peripheral devices. The examiner relies upon such teaching to combine the references.

Conclusion

This is a continuation prosecution. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, [redacted]even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571) 272-4147.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kim Huynh
Primary Examiner
Art Unit 2182

KH
4/26/05